AHUJA COMPENSATION CIRCUIT WITH ENHANCED BANDWIDTH

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to "Frequency Boosting Circuit for High Swing Cascode Biasing Circuits", U.S. Patent Application Serial No. _____, filed _____ (Marvell Docket No. MP0401), which is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to frequency compensation circuits, and more particularly to Ahuja compensation circuits with high swing cascode biasing circuits.

BACKGROUND OF THE INVENTION

[0003] Miller compensation is a conventional frequency compensation technique that involves the movement of a dominant pole of a gain stage to a lower frequency by increasing the effective input capacitance of the gain stage. Miller compensation circuits include a Miller capacitor that exploits the Miller effect. When the Miller capacitor is connected across an input and an output of an amplifier, the capacitance appears much larger from the input of the amplifier. While the dominant pole may be moved to a lower frequency using this approach, bandwidth of the system is still limited.

[0004] Referring now to Figure 1, a Miller compensation circuit 10 includes first and second amplifiers 12 and 14, respectively. An output of the first amplifier 12 communicates with an input of the second amplifier 14. A first end of a first capacitor 16 (or parasitic capacitance) communicates with the input of the second amplifier 14. A first end of a second capacitor 18 (or load capacitance) communicates with an output of the second amplifier 14. Second ends of the first and second capacitors 16 and 18, respectively, communicate with a ground potential 20. A first end of a third capacitor 22 (or compensating capacitance) communicates with the input of the second amplifier 14. A second end of the third capacitor 22 communicates with the output of the second amplifier 14.

[0005] An input voltage 24, v_{in}, of the Miller compensation circuit 10 is applied to an input of the first amplifier 12. An output voltage 26, v_{out}, of the Miller compensation circuit 10 is referenced from the output of the second amplifier 14. The transconductance, g_{m_2}, of the second amplifier 14 may be increased to increase the overall bandwidth.

[0006] Referring now to Figures 2A and 2B, there are two conventional ways to increase the transconductance of the second amplifier 14. In Figure 2A, a voltage gain device 28 is used in the feed forward path to increase the transconductance. An input of the voltage gain device 28 communicates with the first ends of the first and third capacitors 16 and 22, respectively, and the output of the first amplifier 12. An output of the voltage gain device 28 communicates with the input of the second amplifier 14.

[0007] In Figure 2B, a current gain device 30 is used in the feedback path to increase the transconductance. An input of the current gain device 30 communicates with the first end of the third capacitor 22. An output of the current gain device 30 communicates with the output of the first amplifier 12, the input of the second amplifier 14, and the first end of the first capacitor 16. An Ahuja compensation circuit 32 is created by adding the current gain device 30 in the feedback path. A transconductance, g_{m_3}, is associated with the current gain device 30.

[0008] While both the voltage gain device 28 in Figure 2A and the current gain device 30 in Figure 2B increase the transconductance of the second amplifier 14, both arrangements also generate a new pole. Poles tend to limit the bandwidth of a circuit. Therefore, there is a cost associated with increasing the transconductance of the second amplifier 14. In the case of the current gain device 30 in Figure 2B, a pole is generated that is associated with the current gain device 30 and the third capacitor 22. The pole is equal to $\frac{g_{m_3}}{C_m}$, where g_{m_3} is the transconductance of the current gain device 30 and C_m is the capacitance of the third capacitor 22.

[0009] The following discussion sets forth the bandwidth of the circuit in FIG. 2B. In order to derive the bandwidth, an open loop response technique is used. The open loop response technique provides information relating to the bandwidth and maximum achievable bandwidth of a circuit. The DC gain of the open loop response is determined by opening the feedback loop at the output of

the amplifier and attaching a voltage source to one end of the opened feedback loop. The output voltage is sensed at the other end (corresponding to the output of the amplifier) of the opened feedback loop.

[0010] To derive the bandwidth, the DC gain of the open loop response and the first dominant pole P_1 are found. Assuming stable operation, there is only one pole P_1 that is located below a crossover frequency. The crossover frequency is the product of the DC gain of the open loop response and the first dominant pole P_1. The crossover frequency defines the bandwidth of the closed loop amplifier. The maximum available bandwidth is related to the second non-dominant pole P_2.

[0011] Referring now to FIG. 2C, the open loop response of the circuit of FIG. 2B is shown. Initially, the open loop response of the second amplifier stage will be considered. When the open loop response technique is employed, the feedback loop is opened between the capacitance C_m and the output of the second amplifier 14. The input voltage is applied to the disconnected end of the capacitance C_m and the output voltage is taken at the output of the second amplifier 14. At DC, the capacitance is an open circuit. Therefore the gain is usually considered at a mid-frequency as shown in FIG. 2C. The gain at mid-frequency is $g_{m2}R_{o2}\left(\frac{C_m}{C_p}\right)$ and the first dominant pole occurs at $\frac{1}{R_{o2}(C_L+C_m)}$ for the second stage. Multiplying the gain of the open loop response with the dominant pole P_1 results in the crossover frequency of $\frac{g_{m_2}}{C_L+C_m}\left(\frac{C_m}{C_p}\right)$ for the

second stage. Further the second stage has a first non-dominant pole at $\frac{g_{m_3}}{C_m}$, which relates to a barrier frequency or maximum achievable bandwidth.

[0012] The unity bandwidth or crossover frequency of the second stage is equivalent to the first non-dominant pole of the main loop including the first amplifier 12. As described above, the first non-dominant pole defines a barrier frequency or maximum achievable bandwidth of the circuit. Therefore, the circuit in FIG. 2B has a frequency response that is limited to $\frac{g_{m_2}}{C_L + C_m}\left(\frac{C_m}{C_p}\right)$, which is undesirable.

[0013] Referring now to Figure 2D, in one approach, a fourth capacitor 34 that may be added to the Ahuja frequency compensation circuit 32. A first end of the fourth capacitor 34 communicates with the input of the second amplifier 14 and a second end of the fourth capacitor 34 communicates with the output of the second amplifier 14. However, while the arrangement in Figure 2D may be utilized to adjust the non-dominant pole, the non-dominant pole still creates a limitation on the overall bandwidth of the system. The addition of the zero improves the frequency response slightly and alleviates the phase margin of the internal loop.

[0014] Alternatively, the transconductance of the current gain device 30 may be increased to increase the frequency of the non-dominant pole. However, conventional methods for increasing the transconductance of the current gain device 30 usually increase power consumption and/or require additional components.

SUMMARY OF THE INVENTION

[0015] An Ahuja compensation circuit includes first and second transistors and first, second, and third capacitances. A second terminal of the first transistor communicates with a control terminal of the second transistor. A first end of the first capacitance communicates with the second terminal of the first transistor. A first end of the second capacitance communicates with a first terminal of the second transistor. A second end of the third capacitance communicates with the first terminal of the second transistor. A high swing cascode biasing circuit communicates with the second terminal of the first transistor and a first end of the third capacitance. The high swing cascode biasing circuit includes a current biasing circuit that generates a cascode bias and a main bias. A frequency boosting circuit receives the cascode bias and the main bias. A current mirror circuit receives the main bias.

[0016] In other features, feedback is used to increase a transconductance of the high swing cascode biasing circuit. The current mirror circuit comprises third and fourth transistors. A second terminal of the third transistor communicates with a first terminal of the fourth transistor. A first terminal of the third transistor communicates with the control terminal of the second transistor. The second terminal of the third transistor communicates with the first end of the third capacitance.

[0017] In still other features, the current biasing circuit comprises fifth, sixth, seventh, and eighth transistors each having a first terminal, a second terminal, and a control terminal. The second terminals of the fifth and seventh

transistors communicate with the first terminals of the sixth and eighth transistors, respectively. The control terminals of the fifth and sixth transistors communicate. The first terminal of the fifth transistor communicates with the control terminal of the seventh transistor, and the control terminal of the eighth transistor communicates with the first terminal of the seventh transistor.

[0018] In yet other features, control terminals of the third and fourth transistors communicate with the control terminals of the seventh and eighth transistors, respectively. The current biasing circuit further comprises a fourth capacitance having a first end that communicates with the second terminal of the fifth transistor.

[0019] In other features, the frequency boosting circuit comprises a resistance having a first end that communicates with the first terminal of the fifth transistor and a second end that communicates with the control terminal of the fifth transistor. A fourth capacitance has a first end that communicates with the second end of the resistance and a second end that communicates with the second terminal of the third transistor. The first, second, third, fourth, fifth, sixth, seventh, and eighth transistors are metal-oxide semiconductor field-effect transistors (MOSFETs). The resistance is one of a standard fixed-value resistor, a nonlinear resistor, and a metal-oxide semiconductor (MOS) resistor. The first terminals of the fifth and seventh transistors communicate with first and second current sources, respectively. An input voltage of the Ahuja compensation circuit is applied to a control terminal of the first transistor. An output voltage of the

Ahuja compensation circuit is referenced from the first terminal of the second transistor.

[0020] A feedback loop in an Ahuja compensation circuit includes a first transistor and a first capacitance having a first end that communicates with a first terminal of the first transistor. A high swing cascode biasing circuit communicates with a second end of the first capacitance and a control terminal of the first transistor and includes a current biasing circuit that generates a cascode bias and a main bias. A frequency boosting circuit receives the cascode bias and the main bias. A current mirror circuit receives the main bias. The frequency boosting circuit biases the current mirror circuit based on feedback from the current mirror circuit.

[0021] In other features, the current mirror circuit comprises second and third transistors. A second terminal of the second transistor communicates with a first terminal of the third transistor. A first terminal of the second transistor communicates with the control terminal of the first transistor. The second terminal of the second transistor communicates with the first end of the first capacitance.

[0022] In still other features, the current biasing circuit comprises fourth, fifth, sixth, and seventh transistors each having a first terminal, a second terminal, and a control terminal. The second terminals of the fourth and sixth transistors communicate with the first terminals of the fifth and seventh transistors, respectively. The control terminal of the fourth transistor communicates with the control terminal of the fifth transistor. The first terminal of

the fourth transistor communicates with the control terminal of the sixth transistor. The control terminal of the seventh transistor communicates with the first terminal of the sixth transistor.

[0023] In other features, control terminals of the second and third transistors communicate with the control terminals of the sixth and seventh transistors, respectively. The current biasing circuit further comprises a second capacitance having a first end that communicates with the second terminal of the fourth transistor. The frequency boosting circuit comprises a resistance having a first end that communicates with the first terminal of the fourth transistor and a second end that communicates with the control terminal of the fourth transistor. A second capacitance has a first end that communicates with the second end of the resistance and a second end that communicates with the second terminal of the second transistor. The first, second, third, fourth, fifth, sixth, and seventh transistors are metal-oxide semiconductor field-effect transistors (MOSFETs). The resistance is one of a standard fixed-vale resistor, a nonlinear resistor, and a metal-oxide semiconductor (MOS) resistor.

[0024] In still other features, a system comprises the feedback loop and further comprises an Ahuja compensation circuit including the first transistor and a second transistor. A second terminal of the second transistor communicates with the control terminal of the first transistor. An input voltage of the system is applied to a control terminal of the second transistor. An output voltage of the system is referenced from the first terminal of the first transistor.

[0025] In still other features, the Ahuja compensation circuit comprises second and third capacitances. A first end of the second capacitance communicates with the control terminal of the first transistor. The first end of the third capacitance communicates with the first terminal of the first transistor.

[0026] Further areas of applicability of the present invention will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the invention, are intended for purposes of illustration only and are not intended to limit the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The present invention will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0028] Figure 1 is an electrical schematic of a Miller compensation circuit according to the prior art;

[0029] Figure 2A is an electrical schematic of a Miller compensation circuit that includes a voltage gain device in the feed forward path according to the prior art;

[0030] Figure 2B is an electrical schematic of an Ahuja compensation circuit that includes a current gain device in the feedback path according to the prior art;

[0031] Figure 2C illustrates the open loop response of a second amplifier stage for the Ahuja compensation circuit in Figure 2B according to the prior art;

[0032] Figure 2D is an electrical schematic of an Ahuja compensation circuit that includes a capacitor in parallel with an amplifier for adjusting a non-dominant pole according to the prior art;

[0033] Figure 3 is a functional block diagram of an Ahuja compensation circuit that includes a high swing cascode biasing circuit with a frequency boosting circuit according to the present invention;

[0034] Figure 4 is a functional block diagram of the high swing cascode biasing circuit and the frequency boosting circuit of FIG. 3;

[0035] Figure 5A is an electrical schematic of the high swing cascode biasing circuit and the frequency boosting circuit of Figure 4 in further detail;

[0036] Figure 5B is an equivalent circuit of the high swing cascode biasing circuit of Figure 5A that illustrates open-loop and closed-loop responses;

[0037] Figure 5C illustrates the open loop response of the high swing cascode biasing circuit in Figure 5A; and

[0038] Figure 6 is an electrical schematic of an Ahuja compensation circuit that includes the high swing cascode biasing circuit in Figure 5A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0039] The following description of the preferred embodiment(s) is merely exemplary in nature and is in no way intended to limit the invention, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements.

[0040] Referring now to Figures 3 and 4, an Ahuja compensation circuit 42 that utilizes a high swing cascode biasing circuit 44 is shown. In Figure 4, one implementation of the high swing cascode biasing circuit 44 is illustrated in further detail and includes a biasing circuit 52 and a current mirror circuit 54. The biasing circuit 52 generates a cascode bias 56 and a main bias 58. The high swing cascode biasing circuit 44 also includes a frequency boosting circuit 60 that receives the cascode bias 56 and the main bias 58 from the biasing circuit 52. The frequency boosting circuit 60 provides a bias signal 62 to and receives a feedback signal 64 from the current mirror circuit 54. The current mirror circuit 54 also receives the main bias 58 from the biasing circuit 52.

[0041] Referring now to Figure 5A, the biasing circuit 52 includes first, second, third, and fourth transistors 72, 74, 76, and 78, respectively. In this implementation, the first, second, third, and fourth transistors 72, 74, 76, and 78, respectively, are metal-oxide semiconductor field-effect transistors (MOSFETs) that have gates, sources, and drains, although other transistor types may be used. Sources (or second terminals) of the first and third transistors 72 and 76, respectively, communicate with drains (or first terminals) of the second and fourth transistors 74 and 78, respectively. A gate (or control terminal) of the second

transistor 74 communicates with a gate of the first transistor 72. A gate of the fourth transistor 78 communicates with a drain of the third transistor 76, and a drain of the first transistor 72 communicates with a gate of the third transistor 76. The drains of the first and third transistors 72 and 76, respectively, communicate with first and second current sources 84 and 86, respectively. The first and second current sources 84 and 86, respectively, communicate with a supply potential 88. Sources of the second and fourth transistors 74 and 78, respectively, communicate with a ground potential 90.

[0042] The current mirror circuit 54 includes fifth and sixth transistors 92 and 94, respectively. A source of the fifth transistor 92 communicates with a drain of the sixth transistor 94. The gate of the third transistor 76 communicates with a gate of the fifth transistor 92. The gate of the fourth transistor 78 communicates with a gate of the sixth transistor 94. A first end of a first capacitor 96 communicates with the source of the fifth transistor 92. A second end of the first capacitor 96 and a source of the sixth transistor 94 communicate with the ground potential 90. A load current 98 flows into the drain of the fifth transistor 92.

[0043] The frequency boosting circuit 60 includes a second capacitor 100, a third capacitor 102, and a resistor 104. The resistor 104, R_f, is connected between the gate of the first transistor 72 and the drain of the first transistor 72. The gate of the first transistor 72 is capacitively coupled by the second capacitor 100, C_{in}, to an output node 106. For example, the second capacitor 100 may be a metal-insulator-metal (MIM) capacitor, a metal-oxide semiconductor (MOS)

capacitor, or any other type of capacitor. The output node 106 additionally connects the source of the fifth transistor 92, the first end of the first capacitor 96, and the drain of the sixth transistor 94. The third capacitor 102, C_b, has one end that is connected to the source of the first transistor 72 and the drain of the second transistor 74 and an opposite end that is connected to the ground potential 90.

[0044] The second and third capacitors 100 and 102, respectively, function as open-circuits during low frequency operation. Very little current flows to the gates of the transistors during low frequency operation. Therefore, little or no current flows through the resistor 104 and the voltage drop across the resistor 104 is approximately zero.

[0045] The configuration of the first transistor 72 and the resistor 104 in the frequency boosting circuit 60 creates an amplifier with a feedback resistor. A node 108 at the second end of the resistor 104 and the gate of the first transistor 72 is an input to the amplifier. A node 110 at the first end of the resistor 104 and the drain of the first transistor 72 is the output of the amplifier. The feedback path increases the overall bandwidth of the high swing cascode biasing circuit 44.

[0046] The second and third capacitors 100 and 102, respectively, are effectively short circuits during high frequency operation. The third capacitor 102 bypasses the second transistor 74 during high frequency operation. The second capacitor 100 creates a path from the gate of the first transistor 72 to the source of the fifth transistor 92. The third capacitor 102 does not generate an internal

pole. If the frequency boosting circuit 60 is implemented in a differential amplifier, the third capacitor 102 may be omitted.

[0047] Referring now to Figure 5B, an equivalent open loop and closed loop circuit of the high swing cascode biasing circuit 44 of Figure 5A is shown. A dotted line 118 indicates a closed feedback loop. The equivalent circuit includes an inverting amplifier 120. Little or no current enters the inverting amplifier 120 during low frequency operation due to the second capacitor 100 effectively operating as an open circuit.

[0048] During high frequency operation, the second capacitor 100 functions as a short-circuit and current flows to the inverting amplifier 120. The inverting amplifier 120 has an input impedance and an output impedance. The input impedance is equal to $R_{in} = \frac{1}{g_{m_4}}\left(1+\left(\frac{R_f}{R_{out}}\right)\right)$. Since the output impedance of the inverting amplifier is very large, the input impedance is approximately equal to $R_{in} = \frac{1}{g_{m_4}}$.

[0049] A voltage source 122 generates current at an input of the inverting amplifier 120. The current is equal to the voltage divided by the input impedance of the inverting amplifier 120. During high frequency operation, the impedance of the second capacitor 100 becomes very small as compared to the input impedance of the inverting amplifier 120. Therefore, the current that enters the inverting amplifier 120 during high frequency operation is equal to

$\frac{v_{in}}{\left(\frac{1}{g_{m_4}}\right)} = v_{in} g_{m_4}$. A voltage drop across the resistor 104 is equal to $v_{in} g_{m_4} R_f$. This voltage, $v_{in} g_{m_4} R_f$, appears at the output node 106. Current flows from the resistor 104 to the fifth transistor 92. The size of the resistor 104, R_f, is preferably larger than $\frac{1}{g_{m_4}}$.

[0050] Referring now to Figure 5C, the open loop response technique is utilized to characterize the bandwidth of the system. The DC gain of the open loop response is equal to $R_f g_{m_4}$ and a dominant pole occurs at $\frac{g_{m_3}}{C_L}$. Therefore, the crossover frequency is equal to $g_{m_4} R_f \left(\frac{g_{m_3}}{C_L}\right)$. In other words, the pole $\frac{g_{m_3}}{C_L}$ is moved upwards in frequency by the gain $R_f g_{m_4}$. There is also sufficient separation between all other poles and the crossover frequency. When the feedback loop is closed by the second capacitor 100, the transconductance, g_{m_3}, of the fifth transistor 92 is significantly increased.

[0051] Referring now to Figure 6, the high swing cascode biasing circuit 44 is implemented as a current gain device in the Ahuja compensation circuit 42. The Ahuja compensation circuit 42 includes seventh and eighth transistors 123 and 124, respectively. A source of the seventh transistor 123 communicates with a gate of the eighth transistor 124 and the drain of the fifth transistor 92. A drain of the eighth transistor 124 communicates with a third current source 125. The third current source 125 and the drain of the seventh

transistor 123 communicate with the supply potential 88. A first end of a fourth capacitor 126 communicates with the source of the seventh transistor 123. The first end of the first capacitor 96 communicates with the drain of the eighth transistor 124. A second end of the fourth capacitor 126 and a source of the eighth transistor 124 communicate with the ground potential 90. The source of the fifth transistor 92 is coupled by a fifth capacitor 127 to the drain of the eighth transistor 124.

[0052] An input voltage 128, v_{in}, enters a gate of the seventh transistor 123, and an output voltage 130, v_o, is referenced from the output node 106. A node voltage 132, v_1, is referenced from a node between the source of the fifth transistor 92 and the drain of the sixth transistor 94.

[0053] The third capacitor 102 functions effectively as a short circuit during high frequency operation and bypasses the second transistor 74. This prevents an additional pole from occurring in the high swing cascode biasing circuit 44. As discussed above, if the high swing cascode biasing circuit 44 is differential, the third capacitor 102 may be omitted. The Ahuja compensation circuit 42 of the present invention is particularly applicable to analog-to-digital (A/D) applications and regulators. However, those skilled in the art can appreciate that the Ahuja compensation circuit 42 of the present invention is applicable in other circuits.

[0054] Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the present invention can be implemented in a variety of forms. Therefore, while this invention has been

described in connection with particular examples thereof, the true scope of the invention should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of the drawings, specification, and the following claims.